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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) 67,200-1258	
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		First Named Inventor <u>Chen</u>	
		Art Unit <u>2826</u>	Examiner <u>Quach, Tuan N.</u>
Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.			
✓ This request is being filed with a notice of appeal. (Attached) <u>Notice of Appeal (and fees) filed to PTO (by fax) on 1/12/06.</u>			
The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.			
I am the <input type="checkbox"/> applicant/inventor. <input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96) <input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>31,311</u> <input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____		<u>[Signature]</u> Signature <u>Randy TUNG</u> Typed or printed name <u>248-540-4040</u> Telephone number <u>1/20/06</u> Date	
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.			
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PRE-APPEAL BRIEF REQUEST FOR REVIEW

APPELLANTS: Chen et al.

Group Art Unit: 2826

Serial No.: 10,809,974

Examiner: Quach, Tuan N.

Filed: 03/26/2004

In Response to Office Action  
Dated: 12/28/2005For: HIGH-K GATE DIELECTRIC STACK WITH BUFFER LAYER TO IMPROVE  
THRESHOLD VOLTAGE CHARACTERISTICS

Attorney Docket No.: 67,200-1258

CERTIFICATE OF MAILING OR FACSIMILE TRANSMISSION

I hereby certified that this correspondence is (1) ☐ being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to the Commissioner for Patents, P O Box 1450, Alexandria, VA 22313-1450 on January 20, 2006; or (2) ☒ being facsimile transmitted to the United States Patent and Trademark Office at facsimile number (571)-273-8300 January 20, 2006.

Randy W. Tung

Printed Name

Please forward all correspondence to

Signature

1/20/06  
DateTUNG & ASSOCIATES  
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Sir:

Applicants request review of Examiner's final rejection,  
dated 10/20/2005, of claims 22-42 under 35 USC § 103.

**SUMMARY OF CLAIMED SUBJECT MATTER**

The claimed subject matter is directed to a gate structure for a MOSFET device including a novel buffer layer disposed between a high-K dielectric layer and a gate electrode layer (see item 16, Figures 1C; paragraphs 0021-0026) where a buffer dielectric layer is on the high-K gate dielectric and the buffer layer comprises dopants selected from the group consisting of a metal, a semiconductor, and nitrogen; (see Figures 1D-1E; paragraphs 0027-0028; claim 1) as part of a MOSFET device (see Figure 1F; paragraph 0029). Independent claim 41 encompasses the embodiment of a buffer dielectric layer on the high-K gate dielectric and an interfacial layer between the semiconductor substrate and the high-K dielectric layer (see item 14A, Figures 1A-1C; paragraph 0016). Independent claim 42 encompasses the embodiment of a buffer dielectric layer on the high-K gate dielectric and the high-K dielectric layer formed on the semiconductor substrate (see paragraph 0016).

Dependent claims are directed to functional aspects affected by composition (claims 23 and 24) and compositional aspects of the buffer layer (claims 26-40).

Specifically, APPELLANTS overcome the problem of Fermi-level pinning at a high-K gate/gate electrode interface, for example caused by the formation of interface metal-Si bonds. In addition, APPELLANTS

invention including the buffer layer has the beneficial aspects of reducing a Voltage threshold (V<sub>th</sub>) shift compared to the absence of the buffer layer, and preventing interdiffusion of metals, e.g., Si and high-K dielectric gate metals across a gate electrode/high-K gate interface (see Specification paragraphs 005, 0030 and 0031).

Question for Review

The essential question to be reviewed is whether the reference used in rejecting Applicants independent claims, Parker et al., disclose Applicants claimed gate structure: **where a buffer layer is on a high-K gate dielectric layer and a gate electrode layer is on the buffer layer** (see claims 1, 41, and 42). Claim 41 claims a buffer dielectric layer on the high-K gate dielectric and adds an interfacial layer between the high-K gate dielectric and the semiconductor substrate and claim 42 claims a buffer dielectric layer on the high-K gate dielectric and has the high-K gate dielectric on the semiconductor substrate.

Applicants have clearly pointed out the failure of the teachings of the primary reference Parker et al. who clearly only disclose and **teach a buffer layer between the high-K gate dielectric and the semiconductor substrate**, not a buffer dielectric layer on the high-K gate dielectric, and for a different purpose; preventing shorting

of through a thin high-K gate dielectric. The Panel is referred to Applicants response to Examiner in Applicants Request for Reconsideration after Final filed on or about 12/20/2005, e.g., see pages 10-17, reproduced briefly, below:

The buffer layer in the gate structure of Parker et al. (between the semiconductor substrate and the high-K gate dielectric) is taught to be formed for the purpose of **avoiding shorting through a thin gate dielectric** (col 1, lines 35-36). In addition, Parker et al. additionally teach reoxidizing (e.g., col 3, lines 11-15) the high-K dielectric layer **following formation of the high-K dielectric on the buffer layer to improve an interface between the high-K dielectric and the gate electrode** (col 1, lines 38-40; col 2, lines 21-30) **by repairing oxygen vacancies**. In the gate structure of Parker et al., a gate electrode is formed **on the high-K dielectric** following the reoxidation process (col 3, lines 66- 67). In another embodiment the high-K dielectric layer is formed directly on the substrate and the buffer layer formed **between the high-K dielectric and the substrate** (col 4, lines 16-21) **during reoxidation** of the high-K dielectric layer (col 4, lines 38-46), not a buffer dielectric layer on the high-K gate dielectric.

It is therefore respectfully submitted that the Panel of Examiners find that the Final Rejection is improper under the statutory standard of 35 USC § 103(a) since Applicants gate structure has clearly not been shown in the prior art.

Respectfully submitted,

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